comprising the steps of:

forming a crystalline semiconductor film over a substrate;

patterning the crystallized semiconductor film to form first and second semiconductor islands;

forming an insulating film comprising silicon oxide on each of said first and second semiconductor islands by a vapor phase deposition using TEOS;

irradiating an intense light to said insulating film in an atmosphere comprising an oxygen gas; and

forming a gate electrode on said insulating film;

introducing phosphorus into said first and second semiconductor islands; and

introducing boron into said second semiconductor island,

wherein a dose amount of said boron is larger than that of said phosphorus.

REMARKS

The Office Action of **September 17, 2001**, has been received and its contents carefully noted. Applicant respectfully submits that this response is timely filed and fully responsive to the Office Action. Claims 1-14 and 29-37 were pending in the present application prior to the aforementioned amendment. By the above amendment, claims 1, 6, 11, 30, and 34 are amended to more clearly define subject matter which Applicant was already entitled. Because the amended claim language is supported at least on pages 13-17 of the specification and Figures 1A-1E of the drawings, Applicant submits that no issue of new matter is raised by this amendment. Accordingly, claims 1-14 and 29-37 are still pending in the present application and, at least for the reasons set forth below, are believed to be in condition for allowance.

Initially, the Examiner finds that the information submitted in the Information Disclosure Statements filed November 10, 1999 and February 16, 2000 allegedly fail to

comply with 37 C.F.R. §1.98(a)(2), and thus, are not being considered. Applicant traverses this finding in that the information submitted in the IDS of February 16, 2000 was previously acknowledged as considered by the Examiner on March 14, 2001. Appendix A contains a copy of the initialed copy of the Form PTO 1449 of February 16, 2000. Accordingly, the issue regarding the alleged non-compliance with the Rules concerning the IDS of February 16, 2000 should be moot.

With regard to the Information Disclosure Statement filed November 10, 1999, Applicant respectfully contends that this IDS is appropriate under the Rules and, thus, should be considered inasmuch as it falls within the exception to the IDS requirement for copies of the submitted information. M.P.E.P. §609 (August 2001). Specifically, 37 C.F.R. §1.98(d) provides that:

> A copy of any patent, publication, pending U.S. application, or other information listed in an information disclosure statement is not required to be provided if: (1) the information was previously cited by or submitted to, the Office in a prior application, provided that the prior application is properly identified in the IDS and is relied on for an earlier filing date under 35 U.S.C. 120; and (2) the IDS submitted in the earlier application complies with 37 C.F.R. 1.98(a)-(c). If both of these conditions are met, the examiner will consider the information previously cited or submitted to the Office and considered by the Office in a prior application relied on under 35 U.S.C. 120.

Applicant submits that the subject application complies with the first nexus of 37 C.F.R. §1.98(d) since the November 10, 1999 IDS included a statement that the information listed in the Form PTO 1449 was cited in applications relied upon for domestic priority under 35 U.S.C. 120, namely, parent Application Serial No. 08/721,526 (now U.S. Patent No. 6,169,980), and its predecessor, Application Serial No. 08/111,522 (now abandoned). Further, as can be readily seen in Appendix B, each of the cited references in the IDS of November 10, 1999 were either submitted by Applicant or cited by the Office during prosecution of the '980 patent and '522 application.

Applicant further submits that the subject application complies with the second nexus of 37 C.F.R. §1.98(d) since the information contained in the IDS of November 10, 1999 was previously considered by the Office. Appendix B contains initialed copies of Forms PTO 1449 and copies of PTO 892s that were considered by the Office during prosecution of the '980 patent and the '522 application. Accordingly, the fact that each item of information cited in the Form PTO 1449 were initialed by the Office indicates that the IDS's were in conformance with the requirements of 37 C.F.R. §1.98. Consequently, the Examiner is obligated under 37 C.F.R. §1.98(d) to consider the information contained in the IDS of November 10, 1999.

It is not understood why the Examiner would indicate that Applicant's failed to comply with the Rules, when in fact, as the aforementioned argument sets forth, the black letter of the Rules were followed. Applicant understands that the integrity of the PTO filewrappers are sometimes compromised, and for the sake of prosecutorial expediency, Applicant is more than willing to assist the Patent Office in such an occurrence and will submit these copies for the Examiner's convenience, shortly. Applicant should not, however, be cited by the Examiner as being non-compliant with the Rules.

The Office Action maintains the rejections of claims 1-4, 6-9 and 30-33 under 35 U.S.C. §103(a) as unpatentable over ***Applicant's Admitted Prior Art*** (hereinafter "***APA***") in view of either ***Ang et al.*** ("Electrical characterization of low-pressure chemical-vapor-deposited silicon dioxide metal-oxide-silicon structures" Journal of Applied Physics 73(5) pp. 2397-2401, 1 March 1993), claims 1-4, 6-9, 11-13, 29, 30-33 and 34-37 under 35 U.S.C. §103(a) as unpatentable over ***APA*** in view of ***Roy*** (U.S. Patent No. 5,153,701) and ***Wolf*** (Silicon Processing for the VLSI Era, Vol. 1, Lattice Press: Sunset Beach, CA, 1986, pp. 57-58) or ***JP 58-098933***, and claims 5, 10 and 14 under 35 U.S.C. §103(a) as unpatentable over ***APA*** in view of ***Ang et al.*** or ***Roy*** and ***Wolf***, or ***Roy*** and ***JP 58-098933***, and further in view of ***JP 60-187030***.

The claimed invention is directed to a method of manufacturing a semiconductor device, including, *inter alia*, steps of forming a semiconductor film comprising amorphous silicon over a substrate, crystallizing the semiconductor film by irradiating a laser light, patterning the crystallized semiconductor film to form first and second semiconductor islands, forming an insulating film on each of the first and second semiconductor islands by a vapor phase deposition, irradiating an intense light to the insulating film in an atmosphere comprising an oxygen gas, forming a gate electrode on the insulating film, introducing phosphorus into the first and second semiconductor islands, and introducing boron into the second semiconductor island such that a dose amount of the boron is larger than that of the phosphorus.

As the Examiner well knows, three criteria must be met in order to establish a *prima facie* case of obviousness. *M.P.E.P.* §2143 (August 2001). Initially, there must be some teaching, suggestion, or motivation to combine or modify the teachings of the prior art to produce the claimed invention, found either in the references themselves or in the knowledge generally available to a skilled artisan. *In re Fine*, 837 F.2d 1071, 5 USPQ.2d 1596 (Fed. Cir. 1988). Secondly, there must be a reasonable expectation of success. *In re Rhinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976). And lastly, the prior art must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

Applicant respectfully contends that the claims as presently pending define subject matter which is clearly patentably distinct over the prior art of record. More particularly, Applicant respectfully contends that the ***APA***, either alone or in combination with at least one of ***Ang et al.***, ***JP 60-187030***, ***Roy***, ***Wolf***, ***JP-58-098933*** and ***JP 60-187030***, fails to expressly teach or inherently suggest all of the limitations presently set forth in the claimed invention necessary to support a *prima facie* case of obviousness under §103.

Referring now to the rejection, while the Office Action finds that the proposed ***APA*** modifications teaches a method of manufacturing a semiconductor device using various method steps, it is contended that the respective disclosures set forth in the proposed ***APA*** modifications fail to expressly teach or inherently disclose a method of manufacturing a semiconductor device by performing steps that result in the formation of an N-channel thin film transistor and a P-channel thin film transistor, as presently set forth at least in independent claims 1, 6, 11, 30 and 34. In particular, the combined teachings of the proposed ***APA*** modifications fail to provide a method of manufacturing a semiconductor device by introducing phosphorus into first and second semiconductor islands, and introducing boron into the second semiconductor island such that a dose amount of the boron is larger than that of the phosphorus.

Accordingly, since neither of the proposed ***APA*** modifications expressly teaches or implicitly suggests the disclosed features of the present invention, and also fail to recognize the unobvious advantages first proposed by Applicant, Applicant respectfully requests favorable reconsideration and withdrawal of the §103 rejections. Should the Examiner deem that a conference would expedite prosecution of the instant application, the Examiner is hereby invited to telephone the undersigned to arrange such a conference.

Respectfully submitted,

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Registration No. 35,483
NIXON PEABODY LLP
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
(703) 790-9110
(703) 883-0370 FAX

Marked-up copy of amended claims.

1. (Thrice Amended) A method for manufacturing a semiconductor device comprising the steps of:

forming a semiconductor film comprising amorphous silicon over a substrate;

crystallizing said semiconductor film by irradiating a laser light;

patterning the crystallized semiconductor film to form first and second semiconductor islands;

forming an insulating film on [the crystallized semiconductor film] each of said first and second semiconductor islands by a vapor phase deposition; [and]

irradiating an intense light to said insulating film in an atmosphere comprising an oxygen gas [under a pressure of 10 Torr or less.];

forming a gate electrode on said insulating film;

introducing phosphorus into said first and second semiconductor islands; and

introducing boron into said second semiconductor island,

wherein a dose amount of said boron is larger than that of said phosphorus.

6. (Thrice Amended) A method for manufacturing a semiconductor device comprising the steps of:

forming a semiconductor film comprising amorphous silicon over a substrate;

crystallizing said semiconductor film by irradiating a laser light;

patterning the crystallized semiconductor film to form first and second semiconductor islands;

forming an insulating film comprising silicon oxide on [the crystallized semiconductor film] each of said first and second semiconductor islands by a vapor phase deposition; [and]

irradiating an intense light to said insulating film in an atmosphere comprising an oxygen gas [under a pressure of 10 Torr or less.];

forming a gate electrode on said insulating film;

introducing phosphorus into said first and second semiconductor islands; and

introducing boron into said second semiconductor island,

wherein a dose amount of said boron is larger than that of said phosphorus.

11. (Thrice Amended) A method for manufacturing a semiconductor device comprising the steps of:

forming a semiconductor film comprising amorphous silicon over a substrate;

crystallizing said semiconductor film by irradiating a laser light;

patterning the crystallized semiconductor film to form first and second semiconductor islands;

forming an insulating film comprising silicon oxide on [the crystallized semiconductor film] each of said first and second semiconductor islands by a vapor phase deposition using TEOS; [and]

irradiating an intense light to said insulating film in an atmosphere comprising an oxygen gas [under a pressure of 10 Torr or less.];

forming a gate electrode on said insulating film;

introducing phosphorus into said first and second semiconductor islands; and

introducing boron into said second semiconductor island,

wherein a dose amount of said boron is larger than that of said phosphorus.

30. (Thrice Amended) A method for manufacturing a semiconductor device comprising the steps of:

forming a crystalline semiconductor film over a substrate;

patterning the crystallized semiconductor film to form first and second semiconductor islands;

forming an insulating film comprising silicon oxide on [said crystalline semiconductor film] each of said first and second semiconductor islands by a vapor phase deposition; [and]

irradiating an intense light to said insulating film in an atmosphere comprising an oxygen gas [under a pressure of 10 Torr or less.];

forming a gate electrode on said insulating film;

introducing phosphorus into said first and second semiconductor islands; and

introducing boron into said second semiconductor island,

wherein a dose amount of said boron is larger than that of said phosphorus.

34. (Thrice Amended) A method for manufacturing a semiconductor device comprising the steps of:

forming a crystalline semiconductor film over a substrate;

patterning the crystallized semiconductor film to form first and second semiconductor islands;

forming an insulating film comprising silicon oxide on [said crystalline semiconductor film] each of said first and second semiconductor islands by a vapor phase deposition using TEOS; [and]

irradiating an intense light to said insulating film in an atmosphere comprising an oxygen gas [under a pressure of 10 Torr or less.]; and

forming a gate electrode on said insulating film;

introducing phosphorus into said first and second semiconductor islands; and

introducing boron into said second semiconductor island,

wherein a dose amount of said boron is larger than that of said phosphorus.

EXHIBIT A

of February 14, 2000 Sheet 1 of 1

PTO-1449 (Rev. 8-83) U.S. Department of Commerce Patent and Trademark Office

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Attorney Docket N . 0756-2064	Serial N . 09/437,135
Applicant: Shunpei YAMAZAKI et al.	
Filing Date: November 10, 1999	Group:

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date (if appropriate)

FOREIGN PATENT DOCUMENTS

	Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
EK	63-211759	09/02/88	Japan			Abstract	
EK	49-78483	07/29/74	Japan				X

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner Eric Kaiser Dat Consider d 3/14/01

*EXAMINER: Initial if citati n considered, whether or n t citati n is in conf rmanc with MPEP 609; Draw line thr ugh citati n if not in conformance and n t c nsider d. Include c py of this f rm with next c mmunication to applicant.

EXHIBIT B

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Sheet 1 of 1

Form PTO-1449 (Rev. 8-83)	U.S. Department of Commerce Patent and Trademark Office	Attorney Docket No. 0756-1576	Serial No. 08/721,526
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		Applicant: Shunpei YAMAZAKI et al.	
		Filing Date: Sept 26, 1996	Group: 2813

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date (if appropriate)
EK	5,313,075	05/17/94	Zhang et al	—	—	
EK	5,523,240	06/04/96	Zhang et al	—	—	

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	Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
EK	1-238024	09/22/89	Japan	—	—	Abstract	
	2-224253	09/06/90	Japan	—	—	Abstract	
	3-34434	02/14/91	Japan	—	—	Abstract	
	3-132041	06/05/91	Japan	—	—	Abstract	
	4-110470	04/10/92	Japan	—	—	Abstract	
	4-165679	06/11/92	Japan	—	—	Abstract	
	58-98933	06/13/83	Japan	—	—	Abstract	
	60-241269	11/30/85	Japan	—	—	Abstract	
	62-119974	06/01/87	Japan	—	—	Abstract	
EK	63-105970	05/11/88	Japan	—	—	Abstract	
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Examiner	Eric Kielin	Date Considered	8/28/00

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Submitted with IDS of August 8, 2000

Notice of References Cited

Application No.	Applicant(s)		
08/721,526	Yamazaki		
Examiner	Group Art Unit	Page 1 of 1	
Matthew Whipple	2813		

U.S. PATENT DOCUMENTS

		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS
	A	5,970,384	10/99	Yamazaki	438	795
	B					
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

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		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUBCLASS
	N						
	O						
	P						
	Q						
	R						
	S						
	T						

NON-PATENT DOCUMENTS

		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
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	V		
	W		
	X		

Notice of References Cited

Application No.	Applicant(s)		
08/721,526	Yamazaki et al.		
Examiner	Group Art Unit	Page 1 of 1	
Matthew Whipple	2813		

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		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS
X	A	5,773,325	6/98	Teramoto	438	151
X	B	5,237,188	8/93	Iwai	257	325
	C					
	D					
	E					
	F					
	G					
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	I					
	J					
	K					
	L					
	M					

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		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUBCLASS
	N						
	O						
	P						
	Q						
	R						
	S						
	T						

NON-PATENT DOCUMENTS

		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
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	W		
	X		

PTO-1449 (Rev. 8-83) | U.S. Department of Commerce Patent and Trademark Office

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Atty.Docket No.	Serial No.
0756-1576	08/721,526
Applicant: Shunpei YAMAZAKI et al.	
Filing Date: September 26, 1996	Group: 1104

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Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date (if appropriate)
MN		5,705,829	01/06/98	Miyanaga et al.			
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MN		5,756,364	05/26/98	Tanaka et al.			
MN		5,773,327	06/30/98	Yamazaki et al.			

OIPE JUL 14 1998 PATENT & TRADEMARK OFFICE

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		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner	Date Considered
M. Mahadevan	9/17/98

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1449 (83)	U.S. Department of Commerce Patent and Trademark Office	Atty.Docket No. 0756-1576	Serial No. 08/721,526
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		Applicant Shunpei YAMAZAKI et al.	
		Filing Date September 26, 1996	Group 1104

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MW		5,624,851	04/29/97	Takayama et al.			
MW		5,637,515	06/10/97	Takemura			
MW		5,643,826	07/01/97	Ohtani et al.			
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Examiner [signature] Date Considered 9/17/98

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1449 (8-83) U.S. Department of Commerce Patent and Trademark Office		Atty.Docket No. 0756-1576	Serial No. 08/721,526
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		Applicant Shunpei YAMAZAKI et al.	
		Filing Date September 26, 1996	Group 1104

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MW		5,595,923	01/21/97	Zhang et al.			
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MW		5,604,360	02/18/97	Zhang et al.			
MW		5,605,846	02/25/97	Ohtani et al.			
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		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No

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Examiner MWatkins Date Considered 7/17/98

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO-1449 (Rev. 8-83)

U.S. Department of Commerce
Patent and Trademark Office

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Atty.Docket No.	Serial No.
0756-1576	08/721,526
Applicant: Shunpei YAMAZAKI et al.	
Filing Date: September 26, 1996	Group: 1104

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MW		5,589,694	12/31/96	Takayama et al.			

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Examiner MW Date Considered 9/17/98

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Atty.Docket No. 0756-1576	Serial No. 08/721,526
Applicant Shunpei YAMAZAKI et al.	
Filing Date September 26, 1996	Group 1104

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date (if appropriate)
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MW		4,727,044	02/23/88	Yamazaki			
MW		5,010,037	04/23/91	Lin et al.			
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		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
MW		58-190020	11/05/83	Japan			X Ab	
MW		05-58789	03/09/93	Japan			X Ab	
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Examiner MW Date Considered 9/17/98

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PTO-1449 (8-83) | U.S. Department of Commerce Patent and Trademark Office

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Attorney D cket N . 0756-1576	Serial N . 08/721,526
Applicant: Shunpei YAMAZAKI et al.	
Filing Date: Sept. 26, 1996	Gr up: 1104

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date (if appropriate)

FOREIGN PATENT DOCUMENTS

	Document Number	Date	Country	Class	Subclass	Translation Y s	Translation No
	1-149475	06/12/89	Japan			Abstract	
	1-128572	05/22/89	Japan			Abstract	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner [signature] | Date Consider d 9/24/99

*EXAMINER: Initial if citation considered, whether or not citation is in conformanc with MPEP 609; Draw lin thr ugh citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

...tted with IDS of Sept mber 7, 1999 — Sheet 1 of

Form PTO-1449 (Rev. 8-83) U.S. Department of Commerce Patent and Trademark Office	Attorn y D cket No. 0756-1576	Serial No. 08/721,526
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	Applicant: Shunpei YAMAZAKI et al.	
	Filing Date: Sept. 26, 1996	Group: 2813

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date (if appropriate)
MW	5,077,233	12/31/91	Mukai			

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MW	61-89621	05/07/86	Japan			Abstract	
MW	61-166074	07/26/86	Japan			Abstract	
MW	EP 0 178 447	04/23/86	Europe			Full & Abstract	

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Examiner MW — Dat C nsider d 9/29/99

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Form PTO-1449 (Rev. 8-83) — U.S. Department of Commerce, Patent and Trademark Office

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Atty.Docket No.	Serial No.
0756-1576	08/721,526
Applicant	
Shunpei YAMAZAKI et al.	
Filing Date	**Group**
September 26, 1996	1104

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date (if appropriate)
MN		4,851,370	07/25/89	Doklan et al.	437	225	
MN		5,476,802	12/19/95	Yamazaki et al.	437	21	

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
MN		5-55246	08/26/91	JAPAN			ABS	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

MN		C. Hayzelden et al. "In situ transmission electron microscopy studies of silicide-mediated crystallization of amorphous silicon", (3 pages).

Examiner MN Date Considered 8/4/99

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Form PTO-1449 (Rev. 8-83)

U.S. Department of Commerce
Patent and Trademark Office

Atty.Docket No. 0756-1576	Serial No. 08/721,526
Applicant: Shunpei YAMAZAKI et al.	
Filing Date: September 26, 1996	Group: 1104

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date (if appropriate)
MV		4,851,370	07/25/89	Doklan et al.	437	225	
MV		5,476,802	12/19/95	Yamazaki et al.	437	21	

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
MV		5-55246	08/26/91	JAPAN			ABS	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

MV		C. Hayzelden et al. "In situ transmission electron microscopy studies of silicide-mediated crystallization of amorphous silicon", (3 pages).

Examiner: MV Date Considered: 8/4/99

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO-1449 (Rev. 8-83) | U.S. Department of Commerce Patent and Trademark Office | Sheet 1 of 1

INFORMATION DISCLOSURE STATEMENT

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Attorney Docket No. 0756-1576	Serial No. 08/721,526
Applicant: Shunpei YAMAZAKI et al.	
Filing Date: Sept. 26, 1996	Group: 1104

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	5,608,232	03/04/97	Yamazaki et al.	257	66	06/05/95
	5,639,698	06/17/97	Yamazaki et al.	437	228	02/15/94
	5,700,333	12/23/97	Yamazaki et al.	136	258	03/27/96

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Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner: L RADOMSKY

Date Considered: 3/24/98

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Notice of References Cited

Application No.	Applicant(s)		
08/721,526	Yamazaki et al.		
Examiner	Group Art Unit	Page 1 of 1	
Leon Radomsky	1104		

U.S. PATENT DOCUMENTS

	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS
A					
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FOREIGN PATENT DOCUMENTS

	DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUBCLASS
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Application No.	Applicant(s)		
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Examiner		Group Art Unit	Page 1 of 1
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B	5,275,851	1-4-94	Fonash et al.	437	233
C	4,810,673	3-7-89	Freeman	437	239
D	5,225,355	7-6-93	Sugino et al.	437	10
E	5,300,187	4-5-94	Lesk et al.	437	13
F	5,244,819	9-14-93	Yue	437	11
G	4,231,809	11-4-80	Schmidt	----	----
H	RE 28,386	4-8-75	Heiman et al.	----	----
I	RE 28,385	4-8-75	Mayer	----	----
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	DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUBCLASS
N	3-203329	9-91	Japan	Utaka	----	----
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U	Translation of JP 2-140915	5-1990
V	P.H. Robinson et al., J. Electrochem. Soc. 118(1)(1971)141 "Use of HCl gettering in silicon..."	1-1971
W	J.M. Green et al., IBM Tech. Discl. bulletin 16(5)(1973)1612 "Method to purify semiconductor wafers"	10-1973
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Examiner		Group Art Unit	Page 1 of 1
Leon Radomsky		1104	

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		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS
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	N	61-63020	4-1-86	Japan	Horioka, et al.	---	---
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TO SEPARATE, HOLD TOP AND BOTTOM EDGES, SNAP-APART AND D[illegible]D CARBON

FORM PTO-892 (REV. 2-92) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	SERIAL NO.	GROUP ART UNIT	ATTACHMENT TO PAPER NUMBER
NOTICE OF REFERENCES CITED	08/111522	1104	14
	APPLICANT(S) YAMAZAKI et al.		

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*		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
	A	5264383	11/23/93	YOUNG	437	40TFT	6/23/92
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°		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHTS. DWG	PERTINENT PP. SPEC.
	L	2-295111	12/6/90	JAPAN	KOBAYASHI	117	904		
	M	64-25515	1/27/89	JAPAN	Koike et al.	—	—		
	N								
	O								
	P								
	Q								

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R	TRANSLATIONS OF JP 4-102375, 2-148831 AND 1-187814 CITED PREVIOUSLY.
S	K.B. KADYRAKUNOV, et al., PHYS. STAT. SOL., A70, (1982) K15 "... PULSED ANNEALING OF Si-SiO_2 STRUCTURES"
T	D.L. CROSTHWAIT, et al., MRS PROC., FALL 1980, LASER AND ELECTRON-BEAM SOLID INTERACTIONS..., P. 399.
U	T.I. KAMINS et al., Solid St. Electron. 23(1980) 1037 "... LASER ANNEALED INSULATORS ON SILICON"

EXAMINER	DATE
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* A copy of this reference is not being furnished with this office action.
(See Manual of Patent Examining Procedure, section 707.05 (a).)

TO[illegible]ATE, HOLD TOP AND BOTT M EDGES, SNAP-APART AND D[illegible]D CARBON

FORM PTO-892 (REV. 2-92) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	SERIAL NO.	GROUP ART UNIT	ATTACHMENT TO PAPER NUMBER
NOTICE OF REFERENCES CITED	08/111522	1104	11
	APPLICANT(S): YAMAZAKI et al		

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	B	4,894,352	1/16/90	LANE et al	—	—	
	C	5,330,614	7/19/94	AHN	437	915	7/22/92
	D	5,124,014	6/23/92	FOO et al	437	238	
	E	5,302,855	4/12/94	MATSUNO et al	—	—	9/10/91
	F	4,585,492	4/29/86	WEINBERG et al	148	Dig 4	
	G	5,317,236	5/31/94	ZAVRACKY et al	437	173	12/31/91
	H	4,963,503	10/16/90	AOKI et al	437	907	
	I	5,313,076	5/17/94	YAMAZAKI et al	—	—	3/17/92
	J	5,352,291	10/4/94	ZHANG et al	437	173	5/27/92
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	M	02-144831	6/7/90	JAPAN	KOIKE	437	908		
	N	02-189954	7/25/90	JAPAN	ISHII	—	—		
	O	03-133131	6/6/91	JAPAN	DAIKISA	—	—		
	P	01-187814	7/27/89	JAPAN	AOYAMA	148	Dig 90		
	Q	59-70114 22	11/15/84	JAPAN	MUKAI	148	Dig 90		

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EXAMINER	DATE	
Leon Radavsky	11/8/94	1 OF 2

* A copy of this reference is not being furnished with this office action.
(See Manual of Patent Examining Procedure, section 707.05 (a).)